**CS 161 – Design and Architecture of Computer Systems Spring 2019 – Quiz 3**

**NAME (First, Last)** _____

1. You are tasked with evaluating two designs for an L1 data cache. In both designs the block size is 16 bytes and the address is 32 bits.

- Design 1: 32 KB cache, direct mapped.
- Design 2: 64 KB 2-way set associative.

a. Show the number of bits for the byte offset, index and tag fields for each of the two designs.

| | Tag | Index | Byte Offset |
|---|---|---|---|
| **Design 1** | 17 | 11 | 4 |
| **Design 2** | 17 | 11 | 4 |

b. By simulation, you have estimated the miss rate of Design 1, on the target workload, to be 10% and that of Design 2 as 5%. The miss latency, in both cases, is 100 cycles. Compute the CPI increase due to this cache for the target workload? Assume the baseline is an ideal pipeline (CPI=1).

| | Design 1 | Design 2 |
|---|---|---|
| **CPI Increase** | 10 increase (or 11 overall) | 5 increase (or 6 overall) |