CS 161 – Design and Architecture of Computer Systems Spring 2019 – Quiz 1

NAME (First, Last) ____

1. The dynamic instruction count distribution on a set of common benchmarks is shown in the table.

Instruction	Frequency
ALU	40%
Load/Store	40%
Branches	20%

a. Assume processor A has CPI of 2 for ALU instructions, CPI of 5 for Load/Store instructions, and CPI of 1 for Branch instructions. What is the total CPI of this processor?

2*0.4+5*0.4+1*0.2 = 3

b. Now assume processor B which works with our baseline multi-cycle implementation (which we had in multi-cycle slides). What is the CPI for ALU (r-type), Branch, Load, and Store instructions?

ALU (R-type): 4, Branch: 3, Load: 5, and Store: 4

c. What is the total CPI if we use our multi-cycle processor (from part b) to run this benchmark? Assume 20% Load, and 20% Store.

4*0.4 + 3 * 0.2 + 5 * 0.2 + 4 * 0.2 = 4

d. What is the total CPI if we use our single-cycle processor?

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2- **Bonus Question**: Consider the MIPS single-cycle and multi-cycle datapaths from lecture. The datapath supports LW, SW, BEQ, and ADD instructions, and it has the following delays:

```
Read register file      4 ns
Write register file     4 ns
ALU                     3 ns
Read memory (I or D)    5 ns
Write memory (I or D)  10 ns
All other operations    0 ns
```

Single-cycle: slowest instruction defines the cycle time. Although Load is the instruction which uses all 5 steps, but store is slowest instruction (since access latency in memory read is 5, but for memory write is 10) instruction which needs 5 + 4 + 3 + 10 = 22ns. Load executes in 21ns!

Multi-cycle = Slowest step defines the cycle time, which is10ns

What is the **minimum clock period** for the single-cycle and multi-cycle processor (in ns)?