CS161
Assignment-4 Solution

1.1

32-bit = 4 bytes /integer, so 16/4 = 4 32-bit integers.

1.2

`I, J`

1.3

`A[I][J]`

2.1

Address	Tag	Index	Offset	H/M
12 (0000 0011 00)	0000	0011	00	M
720 (1011 0100 00)	1011	0100	00	M
172 (0010 1011 00)	0010	1011	00	M
8 (0000 0010 00)	0000	0010	00	M
764 (1011 1111 00)	1011	1111	00	M
352 (0101 1000 00)	0101	1000	00	M
760 (1011 1110 00)	1011	1110	00	M
56 (0000 1110 00)	0000	1110	00	M
724 (1011 0101 00)	1011	0101	00	M
176 (0010 1100 00)	0010	1100	00	M
744 (1011 1010 00)	1011	1010	00	M
1012 (1111 1101 00)	1111	1101	00	M

2.2

Address	Tag	Index	Offset	H/M
12 (0000 001 100)	0000	001	100	M
720 (1011 010 000)	1011	010	000	M
172 (0010 101 100)	0010	101	100	M
8 (0000 001 000)	0000	001	000	H
764 (1011 111 100)	1011	111	100	M
352 (0101 100 000)	0101	100	000	M
760 (1011 111 000)	1011	111	000	H
56 (0000 111 000)	0000	111	000	M
724 (1011 010 100)	1011	010	100	H
176 (0010 110 000)	0010	110	000	M

744 (1011 101 000)	1011	101	000	M
1012 (1111 110 100)	1111	110	100	M

2.3

C1 Direct Mapped 8 words of data, 1-word block, miss-rate = 100%

Address (Tag Index Offset)	H/M
12 (00000 011 00)	M
720 (10110 100 00)	M
172 (00101 011 00)	M
8 (00000 010 00)	M
764 (10111 111 00)	M
352 (01011 000 00)	M
760 (10111 110 00)	M
56 (00001 110 00)	M
724 (10110 101 00)	M
176 (00101 100 00)	M
744 (10111 010 00)	M
1012 (11111 101 00)	M

C2 Direct Mapped 8 words of data 2-word block, miss rate = 10/12 = 83.33%

Address (Tag Index Offset)	H/M
12 (00000 01 100)	M
720 (10110 10 000)	M
172 (00101 01 100)	M
8 (00000 01 000)	M
764 (10111 11 100)	M
352 (01011 00 000)	M
760 (10111 11 000)	H
56 (00001 11 000)	M
724 (10110 10 100)	H
176 (00101 10 000)	M
744 (10111 01 000)	M
1012 (11111 10 100)	M

C3 Direct Mapped 8 words of data 4-word block, miss rate = 11/12 = 91.67%

Address (Tag Index Offset)	H/M
12 (00000 0 1100)	M
720 (10110 1 0000)	M
172 (00101 0 1100)	M
8 (00000 0 1000)	M
764 (10111 1 1100)	M
352 (01011 0 0000)	M
760 (10111 1 1000)	H

56	(00001 1 1000)	M
724	(10110 1 0100)	M
176	(00101 1 0000)	M
744	(10111 0 1000)	M
1012	(11111 1 0100)	M

C2 has the best miss rate

Total Cycles
C1 12*25+12*2 = 324
C2 10*25+12*3 = 286
C3 11*25+12*5 = 335

2.4

First we must compute the number of cache blocks in the initial cache configurations. For this, we divide 32kB by 4 (for the number of bytes per word) and again by 2 (for the number of words per block). This gives us 4096 blocks and a resulting index field width of 12 bits. We also have a word offset size of 1 bit and a byte offset size of 2 bits. This gives us a tag field size of 32-15=17 bits. These tag bits, along with one valid bit per block, will require 18 * 4096 = 73728 bits of 9216 bytes. The total cache size is then 9216 + 32768 = 41984 bytes.
The total cache size can be generalized to:
total_size = data_size + [(valid_bit_size + tag_size) * blocks] total_size = 41984
data_size = blocks * block_size * word_size
word_size = 4
tag_size = 32 - log2(blocks) - log2(block_size) - log2(word_size) valid_bit_size = 1
Increasing from 2-word blocks to 16-word blocks will reduce the tag size from 17 bits to 14 bits. In order to determine the number of blocks, we solve the inequality:
41984 <= (64 * blocks) + (15 * blocks) = 531 blocks Rounding to the next power of 2 gives us a 1024-block cache.
The larger block size may require an increased hit time and an increased miss penalty than the original cache. The fewer number of blocks may cause a higher conflict miss rate than the original cache.

3.1
8

3.2
32

Word Address		Tag {31-10]			Index [9-5]			Offset [4-0]				Cache Index, Tag							
b_{10}	b_2	b_2	b_{10}	b_{16}	b_2	b_{10}	b16	b_2	b_{10}	b_{16}	H/M	0	1	2	3	4	5	6	7
0	0000 0000 0000 0000 0000 0000 0000 0000	0000 0000 0000 0000 0000 00	0	0x0	00 000	0	0x0	0 0000	0	0x00	M	i(0), t(0)							
4	0000 0000 0000 0000 0000 0000 0000 0100	0000 0000 0000 0000 0000 00	0	0x0	00 000	0	0x0	0 0100	4	0x04	H	i(0), t(0)							
16	0000 0000 0000 0000 0000 0000 0001 0000	0000 0000 0000 0000 0000 00	0	0x0	00 000	0	0x0	1 0000	16	0x10	H	i(0), t(0)							
132	0000 0000 0000 0000 0000 0000 1000 0100	0000 0000 0000 0000 0000 00	0	0x0	00 100	4	0x4	0 0100	4	0x04	M	i(0), t(0)				i(4), t(0)			
232	0000 0000 0000 0000 0000 0000 1110 1000	0000 0000 0000 0000 0000 00	0	0x0	00 111	7	0x7	0 1000	8	0x08	M	i(0), t(0)				i(4), t(0)			i(7), t(0)
160	0000 0000 0000 0000 0000 0000 1010 0000	0000 0000 0000 0000 0000 00	0	0x0	00 101	5	0x5	0 0000	0	0x00	M	i(0), t(0)				i(4), t(0)	i(5), t(0)		i(7), t(0)
1024	0000 0000 0000 0000 0000 0100 0000 0000	0000 0000 0000 0000 0000 01	1	0x1	00 000	0	0x0	0 0000	0	0x00	M/R	i(0), t(1)				i(4), t(0)	i(5), t(0)		i(7), t(0)
30	0000 0000 0000 0000 0000 0000 0001 1110	0000 0000 0000 0000 0000 00	0	0x0	00 000	0	0x0	1 1110	30	0x1E	M/R	i(0), t(0)				i(4), t(0)	i(5), t(0)		i(7), t(0)
140	0000 0000 0000 0000 0000 0000 1000 1100	0000 0000 0000 0000 0000 00	0	0x0	00 100	4	0x4	0 1100	12	0x0 C	H	i(0), t(0)				i(4), t(0)	i(5), t(0)		i(7), t(0)
3100	0000 0000 0000 0000 0000 1100 0001 1100	0000 0000 0000 0000 0000 11	3	0x3	00 000	0	0x0	1 1100	28	0x1 C	M/R	i(0), t(3)				i(4), t(0)	i(5), t(0)		i(7), t(0)
180	0000 0000 0000 0000 0000 0000 1011 0100	0000 0000 0000 0000 0000 00	0	0x0	00 101	5	0x5	1 0100	20	0x14	H	i(0), t(3)				i(4), t(0)	i(5), t(0)		i(7), t(0)
2180	0000 0000 0000 0000 0000 1000 1000 0100	0000 0000 0000 0000 0000 10	2	0x2	00 100	4	0x4	0 0100	4	0x04	M/R	i(0), t(3)				i(4), t(2)	i(5), t(0)		i(7), t(0)

3.3
4

3.4

4/12 = 0.33

3.5

<00000_2, 0000 0000 0000 0000 0000 11_2, mem[3100]>

<00100_2, 0000 0000 0000 0000 0000 10_2, mem[2180]>

<00101_2, 0000 0000 0000 0000 0000 00_2, mem[180]>

<00111_2, 0000 0000 0000 0000 0000 00_2, mem[232]>

4.1

3-way 2-word block (8-byte block), total size = 24 words, or 4 sets

Address (Tag Index Offset)	H/M
12 (00000 01 100)	M
720 (10110 10 000)	M
172 (00101 01 100)	M
8 (00000 01 000)	H
764 (10111 11 100)	M

352 (01011 00 000)	M
760 (10111 11 000)	H
56 (00001 11 000)	M
724 (10110 10 100)	H
176 (00101 10 000)	M
744 (10111 01 000)	M
1012 (11111 10 100)	M

Final content with tag bits shown

Set	Way 1	Way 2	Way 3
00	01011		
01	00000	00101	10111
10	10110	00101	11111
11	10111	00001	

4.2

fully associative 1-word block (4-byte block), total size = 8 words, No index bits

Address (Tag Index Offset)	H/M
12 (00000011 00)	M
720 (10110100 00)	M
172 (00101011 00)	M
8 (00000010 00)	M
764 (10111111 00)	M
352 (01011000 00)	M
760 (10111110 00)	M
56 (00001110 00)	M
724 (10110101 00)	M
176 (00101100 00)	M
744 (10111010 00)	M
1012 (11111101 00)	M

Final content with tag bits shown

	Way 1	Way 2	Way 3	Way 4	Way 5	Way 6	Way 7	Way 8
	10110101	00101100	10111010	11111101	10111111	01011000	10111110	00001110

4.3

fully associative 2-word block (8-byte block), total size = 8 entries, No index bits

Address (Tag Index Offset)	H/M
12 (0000001 100)	M
720 (1011010 000)	M
172 (0010101 100)	M
8 (0000001 000)	H
764 (1011111 100)	M

352 (0101100 000)	M
760 (1011111 000)	H
56 (0000111 000)	M
724 (1011010 100)	H
176 (0010110 000)	M
744 (1011101 000)	M
1012 (1111110 100)	M

Final content with tag bits shown

	Way 1	Way 2	Way 3	Way 4	Way 5	Way 6	Way 7	Way 8
	0000001	1011010	1111110	1011111	0101100	0000111	0010110	1011101

5.1

Worst case is $2^{(43-12)}$ entries, requiring $2^{(43-12)}$ * 4 bytes - 2^{33} bytes = 8 GB

5.2

With only 2 levels, the designer can select the size of each page table segment. In a multi-level scheme, reading a PTE requires an access to each level of the table.

5.3

It would be invalid if it was paged out to disk.

5.4

A write to page 30 would generate a TLB miss.

5.5

When an instruction writes to VA page 200, an interrupt would be generated because the page is marked as read only.