

CS161 - Homework 1
DUE Monday, April 29, 2019 IN CLASS!

A) Performance Evaluation:

1- Your job is to evaluate the potential performance of two processors, each implementing a different ISA. The evaluation is based on its performance on a particular benchmark. On the processor implementing ISA A, the best compiled code for this benchmark performs at the rate of 10 IPC. That processor has a 500 MHz clock. On the processor implementing ISA B, the best compiled code for this benchmark performs at the rate of 2 IPC. That processor has a 600 MHz clock.

- a. What is the performance in Millions of Instructions per Second (MIPS) of the processor implementing ISA A?
- b. What is the performance in MIPS of the processor implementing ISA B?
- c. Which is the higher performance processor: A? B? Or Don't know? Briefly explain your answer.

2- Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5, P2 has a 2.5 GHz clock rate and a CPI of 1.0, and P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

- a. Which processor has the highest performance expressed in instructions per second?
- b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions for each processor.
- c. For processor P1, we are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

3- Consider two different implementations of the same instruction set architecture (ISA). The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz have CPIs of 1, 2, 3, and 3 for each class, respectively. P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2 for each class, respectively.

Given a program with a dynamic instruction count of 1,000,000 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

- a. What is the global CPI for each implementation?
- b. Find the clock cycles required in both cases.

4- Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of $1.0E9$ and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of $1.2E9$ and an execution time of 1.5 s.

- Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
- Assume the compiled programs run on two different processors (compiled program A runs on processor A, compiled program B runs on processor B). If the execution times on the two processors are the same, how much faster is the clock of processor A versus the clock of processor B?
- A new compiler is developed that uses only $6.0E8$ instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

5- Memory operations currently take 30% of execution time of program A. A new widget called a “cache” speeds up 80% of memory operations by a factor of 4. A second new widget called a “L2 cache” speeds up half of the remaining 20% by a factor of 2. What is the total speed up?

B) MIPS ISA:

Tip: While you are not expected to memorize all of the assembly instructions, the key skill necessary is to be able to look up MIPS references (or Google ;-) and understand the operation.

6- For the MIPS assembly instructions below, what is the corresponding C statement? Assume that the variables *f*, *g*, *h*, *i*, and *j* are assigned to registers $\$s0$, $\$s1$, $\$s2$, $\$s3$, and $\$s4$, respectively. Assume that the base address of the arrays *A* and *B* are in registers $\$s6$ and $\$s7$, respectively. *sll* is shift left logical, and is an I-type instruction.

```
sll  $t0, $s0, 2      # $t0 = f * 4
add  $t0, $s6, $t0    # $t0 = &A[f]
sll  $t1, $s1, 2      # $t1 = g * 4
add  $t1, $s7, $t1    # $t1 = &B[g]
lw   $s0, 0($t0)      # f = A[f]
addi $t2, $t0, 4
lw   $t0, 0($t2)
add  $t0, $t0, $s0

sw   $t0, 0($t1)
```

7- Translate the following C code to MIPS. Assume that the variables *f*, *g*, *h*, *i*, and *j* are assigned to registers $\$s0$, $\$s1$, $\$s2$, $\$s3$, and $\$s4$, respectively. Assume that the base address of the arrays *A* and *B* are in registers $\$s6$ and $\$s7$, respectively. Assume that the elements of the arrays *A* and *B* are 4-byte words.

```
B[8] = A[i] + A[j];
```

8- Translate the following MIPS code to C. Assume that the variables *f*, *g*, *h*, *i*, and *j* are assigned to registers $\$s0$, $\$s1$, $\$s2$, $\$s3$, and $\$s4$, respectively. Assume that the base address of the arrays *A* and *B* are in registers $\$s6$ and $\$s7$, respectively.

```
addi $t0, $s6, 4
add  $t1, $s6, $0
sw   $t1, 0($t0)
lw   $t0, 0($t0)
```

```
add  $s0, $t1, $t0
```

9- Assume $\$t0$ holds the value $0x00101000$. What is the value of $\$t2$ after the following instructions? *slt* is set less than.

```
    slt  $t2, $0, $t0
    bne  $t2, $0, ELSE
    j    DONE
ELSE: addi $t2, $t2, 2
```

```
DONE:
```